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MID PREP

ISRO

DELTA-SIGMA ASIC Development

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Introduction

Advanced futuristic technologies pertaining to Communication, Navigation, Remote Sensing and Human Spaceflight are major thrust for innovation at SAC. Design and development of Indigenous VLSI circuits like ASICs, SoCs, Photonic-Integrated Circuits is need of hour and national goal of Atmanirbhar Bharat by year 2047. SAC is a leading centre in India for core research and Innovations in VLSI circuit design domain and many ASICs/ SoCs are being developed for various payloads needs. Many of these payloads require high precision temperature, position control with very fine resolution and wide dynamic range. In order to carry out these functions a Delta-Sigma Analog to Digital Converter (ADC) with digitization ranging from 16-24 bits are planned; for usage as ASIC and as a component in a SoC. Involvement of IITs in initial system studies and hardware architecture exploration of this ADC will aid this development.

About Us

Space Applications Centre (SAC) is a major research and development centre of the Indian Space Research Organisation (ISRO), situated at Ahmedabad. Its primary function is design and development of space-borne and air-borne instruments/payloads for ISRO missions; alongside the development and operationalization of space technology applications for societal benefit. These developments and applications encompass critical domains such as communication, broadcasting, navigation, disaster monitoring, meteorology, oceanography, environmental monitoring and natural resource surveying; using microwave remote sensing, optical remote sensing, communication and navigation payloads.

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Furthermore, the centre plays a pivotal role in India's scientific and planetary missions; including Chandrayaan-1, Chandrayaan-2, Chandrayaan-3 Landing mission, Aditya-L1, Mars Orbiter Mission; upcoming missions like Chandrayann-4, Venus Orbiter Mission, Crew Communication & Cabin systems for Gaganyaan. SAC is also developing advanced technologies pertaining to many fields like Quantum Communication, Atomic Clocks.

SAC has state-of-the-art electronic and mechanical design/fabrication facilities; software computing infrastructure for image processing and analysis; software and hardware based applications development for remote sensing, communication and navigation signals/data. SAC partners with industry for sourcing, indigenization & technology transfers, engages Indian universities with collaborative research programs and propagates space technology and applications amongst students and public.

Problem Statement Description

Delta-Sigma ADCs offer the most effective architecture for achieving high-resolution, power-efficient analog-to-digital conversion. These ADCs generally have trade-offs between sampling rate and Effective Number of Bits (ENOB), where higher ENOBs are typically achieved at lower Nyquist sampling rates, and vice versa

The goal of the project (problem statement) is study, simulation and HDL design (digital filter) of Delta-sigma ADC converter. The objective is to achieve higher ENOBs at higher sampling rates by incorporating a suitable Delta-sigma modulator and Digital/ Decimation filter architecture and their order/taps.

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The study shall explore different modulator types (discrete-time, continuous-time, and hybrid) and digital/decimation filter types (e.g., SINC, IIR, FIR). A few types shall be selected for modelling and simulation of a 20-bit Delta-Sigma ADC.

Trade-off simulation studies between Nyquist sampling rate and ENOBs shall be done. Target Nyquist sampling frequencies are between 0.5 ksps to 2 ksps (or wider range) and ENOBs range is from 16 to 19 bits

A digital/decimation filter (equivalent to MATLAB/ Simulink model) shall be designed and implemented at Register Transfer Level (RTL) using Verilog/ VHDL; to be simulated and followed by ASIC design flow steps such as synthesis, layout, and post-layout simulation.

Methodology

Following methodology may be followed to meet and fulfil the objectives.

1. Study of various Delta-Sigma Modulator types like discrete time, continuous time, hybrid; Study of Various Digital/Decimation filter types like SYNC/IIR/ FIR filters; modelling and simulation using MATLAB/ Simulink to achieve >16 ENOBs at various Nyquist sampling rates (i.e. Trade-off analysis between Nyquist sampling rate and ENOB).
2. Study and analysis of effect of flicker noise on ENOB. MATLAB/ Simulink analysis may be done to find out whether chopping will be able to address flicker noise or whether nested chopping or a combination of auto-zeroing and chopping will be required to achieve the high ENOB.

3. Selection of proper quantization bits for Digital Filter/Decimation filter coefficients and order/taps for implementation in Verilog/ VHDL design and analysis w.r.t. floating point model of MATLAB/ Simulink.
4. Design and Simulation of Register Transfer Level (RTL) Verilog/ VHDL Code of Digital/ Decimation filter
5. Synthesis, layout and post-layout Simulation of on digital/decimation filter RTL design

Software

- MATLAB/Simulink
- VCS/QuestaSim or any VHDL/Verilog design simulation platform
- Synopsys Design Compiler or Cadence Genus for Synthesis
- Synopsys ICC/ICC2 or Cadence Innovus for Place and Route
- PDK: SCL/UMC 180 nm or any other available PDK

Evaluation

1. Study, modelling and simulation (35%)
2. RTL design and simulation of selected digital filter architecture (35%)
3. ASIC synthesis and chip layout design (10%)
4. ASIC Post-layout simulation (10%)
5. Presentation (10%)

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Resources

- Hing-Kit Kwan, et al., "Design of hybrid continuous-time discrete-time delta-sigma modulators," 2008 IEEE International Symposium on Circuits and Systems (ISCAS), 2008.
- Analog Devices, “ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications,” Analog Devices Technical Tutorial, 2008, tutorial MT-023.
- S. Ho, C. -L. Lo, J. Ru and J. Zhao, "A 23 mW, 73 dB Dynamic Range, 80 MHz BW Continuous-Time Delta-Sigma Modulator in 20 nm CMOS," in IEEE Journal of Solid State Circuits, vol. 50, no. 4, pp. 908-919, April 2015.